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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,670	01/04/2001	Stuart F. Oberman	5989-00200	5292

7590 07/12/2005

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EXAMINER	
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ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/755,670	OBERMAN ET AL.	
	Examiner	Art Unit	
	Steven HD Nguyen	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16,17,19-44 and 47-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,16,17,19-44,47,48,51,52 and 55-65* is/are rejected.

7)☒ Claim(s) *49,50 and 53* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 14 and 55-65 objected to because of the following informalities:

Claims 61-64, line 12, 14 and 17, "the means" should be replaced with -- the routing means --.

Claims 14 and 64-65, line 14, 16, and 19, "the means" should be replaced with -- the routing means --.

Claims 55-60, "first input port" should be changed to – input port --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 14, 16-17, 19-40 and 55-60 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 recites the limitation "the memory" in lines 8-9.

Claim 14 recites the limitation "the shared memory" in line 19 and 22.

Claims 55-59 recite the limitation "the memory" in lines 5-6.

Claims 55 and 58-60 recite the limitation "the shared memory" in line 16 and 18.

Claim 56 recites the limitation "the shared memory" in line 18 and 20.

Claim 57 recites the limitation "the shared memory" in line 16, 18 and 21.

Claim 57, line 22, "memory" is vague and indefinite because it's unclear which memory the applicant is referred to above. Please clarify, so the meter and boundary of the claim can be determined.

Claim 58 recites the limitation "the shared memory" in line 18 and 20.

There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 1-5, 10, 12-14, 16, 22-23, 28-29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hochschild (USP 5546391) in view of Bass (USP 6144668) and Holt (USP 5790545).

Regarding claims 1 and 13, Hochschild discloses a method for switching packets in a network switch, the method comprising receiving data forming a packet, wherein the packet is to be routed to at least one destination output port of a plurality of output ports includes FIFO (Fig 3, Ref 380) that are part of the network switch (Fig 3, Ref 251); determining whether the destination output port has sufficient resources available to handle the data without causing an overflow (Col. 15, lines 24-57); by request cut through routing from the destination out port in response to receiving data and conveying a signal grant cut through to the source input port if the destination output port has sufficient resource available to handle data; routing the data to the

destination output port if receiving the grant signal (Col. 12, lines 48 to col. 13, lines 44); and if sufficient resources are not available; storing the data to a random access memory (Col. 13, lines 45-51); transferring the data from the random access memory to the destination output port if receiving a not grant signal and waiting until the destination output port has sufficient resources available and transferring the data from the RAM to the output port (Col. 14, lines 57-59). However, Hochschild fails to disclose the input and output ports have a different rate and input port configured to store packet identifier in the output port includes queues. In the same field of endeavor, Bass discloses a switch comprising a plurality input and output ports which routes the data packets based on store and forward or cut through mode (Fig 2, Ref 55 has a speed 1GBps and Ref 45 has speed of 100 Mbps, Fig 3, Ref 206 for store and forward or cut through mode decision). However, Hochschild and Bass fails to disclose the output port includes a plurality of queues to allow the input port to store the packet tags before forwarding the packet to the output port. In the same field of endeavor, Holt discloses a switch includes input port configured to store a packet tag in one of output port queues (Col. 5, lines 20-25).

Since Hochschild suggests that the switch which includes buffer at input port for allowing the upstream circuit and crossbar switch to operate at different speed. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a method for configuring the input port for storing the packet tag in one of output port queues as disclosed by Holt into an input and output ports into a switch that have a different speed as disclosed by Bass into Hoshschild's method and system. The motivation would have been to provide a simultaneous cut through and store and forward frame in a network device to improve transmission delay.

Regarding claim 14, Hochschild discloses (Figs 1,10 and col. 1, lines 12 to col. 28, lines 17) a network switch (Fig 3) comprising a plurality of input ports configured to receive data forming one or more packets (Fig 3A, Ref 310); a plurality of output ports configured to convey the packets out of the switch (Fig 3A, 380); a random access memory (Fig 3A, Ref 350); and data transport logic coupled between the input ports, the output ports, and the memory (Fig 3A, Ref 315, 312, 360), wherein a first input port is configured to request cut-through routing from at least one destination output port in response to receiving data corresponding to a first packet that is a candidate for cut-through routing, wherein the destination output port is configured to convey a signal granting cut-through to the first input port if the destination output port has sufficient resources available to handle the data corresponding to the first packet, wherein, in response to receiving the grant cut-through signal, the input port is configured to route the data corresponding to the first packet to the destination output port via the data transport logic (Col. 12, lines 47 to col. 13, lines 44, the input port receives a packet and generates a request for forwarding the packet to output port. After receiving a grant signal from output port, the receiver will route the packet via a crosspoint switch to the output port by bypass the central queue), and wherein in response to not receiving the grant cut-through signal, the input port is configured to store the data to the shared memory via the data transport logic (Col. 13, lines 45-51, the input port does not receive a grant signal will forward the packet to the central queue), wherein the output port is configured to read the data corresponding to the first packet from the shared memory via the data transport logic in response to having resources available for the data corresponding to the first packet (Col. 13, lines 52-64, the output port will read the stored data in the central queue when it is available; col. lines 57-59). However, Hochschild fails to disclose

the input and output ports have a different rate and input port configured to store packet identifier in the output port includes queues. In the same field of endeavor, Bass discloses a switch comprising a plurality input and output ports which routes the data packets based on store and forward or cut through mode (Fig 2, Ref 55 has a speed 1GBps and Ref 45 has speed of 100 Mbps, Fig 3, Ref 206 for store and forward or cut through mode decision). However, Hochschild and Bass fails to disclose the output port includes a plurality of queues to allow the input port to store the packet tags before forwarding the packet to the output port. In the same field of endeavor, Holt discloses a switch includes input port configured to store a packet tag in one of output port queues (Col. 5, lines 20-25).

Since Hochschild suggests that the switch which includes buffer at input port for allowing the upstream circuit and crossbar switch to operate at different speed. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a method for configuring the input port for storing the packet tag in one of output port queues as disclosed by Holt into an input and output ports into a switch that have a different speed as disclosed by Bass into Hoshschild's method and system. The motivation would have been to provide a simultaneous cut through and store and forward frame in a network device to improve transmission delay.

Regarding claims 2-3, Hochschild implicitly discloses said routing is started before said receiving is complete to implement cut-through routing or early forwarding (the message is routed when input FIFO receives 8 byte message from the link wherein chunk is used for wormhole routing "cut through").

Regarding claim 4, Hochschild implicitly discloses said reading is started after said storing is complete to implement store and forward routing (Central queue stores the message packet if the output port is not available in order to implement store and forward routing).

Regarding claim 5, Hochschild discloses said routing is performed without storing the data in an intervening random access memory (col. 13, lines 19-20).

Regarding claim 10, Hochschild discloses said transferring the data from the random access memory to the destination output port is performed once for each output port that is a destination for the packet (Col. 14, lines 58-60).

Regarding claim 12, Hochschild discloses said storing comprises allocating clusters to the data, wherein each cluster comprises one or more cells, wherein each cell comprises a number of bytes equal to the width of the random access memory's interface (Col. 4, lines 29-47, memory interface is 8 byte width, Chunk reads on cell).

Regarding claim 16, Hochschild discloses each input port comprises an input port FIFO, wherein each output port comprises an output FIFO, wherein the input FIFO is configured to store received data until the received data is routed to the output FIFO or the random access memory (Fig 1, Ref 350 is memory and Ref 410 is input FIFO and Ref 420 is output FIFO for using to store the data).

Regarding claim 22, Hochschild discloses the input port is configured to store the data to the shared memory via the data transport logic in cells (Col. 4, lines 29-47, memory interface is 8 byte width, Chunk reads on cell).

Regarding claim 23, Hochschild discloses the input port is configured to allocate one or more clusters for each received packet, wherein each cluster comprises one or more cells,

wherein each cell equals the size of the random access memory's interface (Col. 4, lines 29-47, memory interface is 8 byte width, Chunk reads on cell).

Regarding claims 28-29, Hochschild discloses the data transport logic includes a cross-bar switch configurable to route data from each input port to each output port and prevent data from a particular input port being routed back to the particular input port. (Fig 3a, Ref 360).

Regarding claim 31, Hochschild discloses the packets have variable lengths (Col. 10, lines 26-41).

19. Claims 6-9, 24-25, 32-37 and 39 rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshschild and Bass as applied to claims 1 and 14 above, and further in view of Herring (USP 6542502).

Regarding claims 6 and 7, Hochschild and Bass fail to fully disclose the claimed invention. However, the examiner take official notice that a method and system for storing the data received in the destination output port in an output first in first out memory (FIFO); and determining whether the output FIFO has a predetermined amount of available storage space before performing said storing, wherein said predetermined amount of available storage space is stored in a programmable register and is a function of the maximum packet size is well known and expected in the art at the time of invention was made to apply a method of determining if the available buffer space before storing or discard the information in order to reduce the processing time of the buffer.

Regarding claim 8, Hochschild and Bass fail to fully disclose the claimed invention. However, the examiner take official notice that a method and system for creating and storing a packet descriptor for the packet, wherein the packet descriptor is stored in a linked list is well

known in the art at the time invention was made to apply a linked list in order to link the sequence of the received packet and performing first in first out. The motivation would have been to maintain the sequence of transmitting packet.

Regarding claim 9, Hochschild and Bass fail to disclose said routing the data is performed to all output ports simultaneously that are destinations for the packet and that have sufficient resources available. In the same field of endeavor, Herring discloses a method and apparatus for routing data simultaneously to the destination ports that have available resources (See col. 4, lines 25-38).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a method and system for replicating a packet from input port to the output ports simultaneously as disclosed by Herring's system and method into Bass and Hochschild's system. The motivation would have been to prevent a dead lock in the system.

Regarding claims 24-25, Hochschild and Bass fail to fully disclose each output port comprises an output FIFO, wherein each output port is configured to refrain from conveying the signal granting cut-through in response to the output port's output FIFO having less than a predetermined number of bytes of available storage or being more than a predetermined percentage full. However, Hochschild discloses when FIFO or Queue has no space to store the chunk; the chunks will not be transmitted from input FIFO or central queue to the output FIFO (See col. 41-52). Therefore, it would have been obvious to one of ordinary skill in the art to implement a method and system for prevent the output port to generate a grant signal when the buffer space is less than a threshold into Bass and Hoshschild's in order to prevent data loss

because this method and system is well known and expected in the art. The motivation would have been to maintain integrity of the packet.

Regarding claims 34-37 and 39, Hochschild and Bass fail to disclose said switch is configurable to disable cut-through routing or early forwarding on a port-by-port basis or a packet-by-packet basis or selectively disable cut-through operations from a particular type of input port to a particular type of output port. However, the examiner takes an official notice that a method and system for disabling cut through based on port, packet are well known and expected in the art such as disable cut through based on packet by packet to prevent packet error, port in order to prevent an over load on an output port when input port is high speed than the input port are well known and expected in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to apply disable cut-through routing or early forwarding into Bass and Hoshschild's system in order to prevent data loss.

Regarding claims 32-33, Hochschild fails to disclose said input port is configured to generate a packet descriptor for each received packet, wherein the packet descriptor comprises at least the length of the corresponding packet and an identifier that identifies the corresponding output port to which the packet is to be routed and an indication of the packet's priority. However, the examiner takes official notice that a method and system for generating a descriptor which includes priority, identify and length is well known and expected in the art at the time of invention was made to create a list for using to read data from buffer in order to prevent a dead lock.

20. Claims 11 and 30 are rejected under 35 U.S.C. 103(a) as being obvious over Hoshschild and Bass as applied to claims 1 and 14 above, and further in view of Dziadosz (USP 5832222).

Regarding claims 11 and 30, Hochschild and Bass fails to disclose the claimed invention. However, Dziadosz discloses said switching the packet comprises encapsulating the packet in a Storage Over IP (SOIP) packet if the packet is a Fibre Channel packet and the output port is an Ethernet port and a network processor for each input port and each output port, wherein said network processors are configured to add an Ethernet prefix to packets in response to detecting that the packets are Fibre Channel packets and are being routed to Ethernet output ports (Fig 2, Ref 28 is a fibre channel port and Ref 16 and 18 are Ethernet port which receives the packet from fibre channel and encapsulating it before transmitting via Ethernet port and col. 8, lines 8-18).

Since Bass suggests FDDI network. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a packet processor in each input/output port for encapsulating Fibre packet into Ethernet Packet as disclosed by Dziadosz's system into Bass and Hochschild's system. The motivation would have been to use the Ethernet network for conveying the Fibre channel packet.

21. Claims 19-21 and 26-27 are rejected under 35 U.S.C. 103(a) as being obvious over Hoshschild and Bass as applied to claims 1 and 14 above, and further in view of Egbert (USP 6091707).

Regarding claims 19-21 and 26-27, Hochschild and Bass fails to disclose the claimed invention. However, Egbert discloses a method and system for preventing an underrun of a memory by setting a threshold value for each port based on transmitting rate in order to compare with the amount stored data before transferring the data (Fig 4 and Col. 11, lines 25-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a method for preventing an underrun of a memory by setting a

threshold value in order to compare with the amount stored data before transferring the data as disclosed by Egbert into Hochschild and Bass. the motivation would have been to improve the throughput of the network.

22. Claim 40 is rejected under 35 U.S.C. 103(a) as being obvious over Hoshschild and Bass as applied to claim 14 above, and further in view of Teitenberg (USP 6421769).

Regarding claim 40, Hochschild and Bass fail to disclose the claimed invention. However, Teitenberg discloses the input ports are either Fibre Channel or Gigabit Ethernet, and wherein the output ports are either Fibre Channel or Gigabit Ethernet (Fig 1 wherein I/O ports are either Ethernet or Fibre channel, See col. 2, lines 1-17).

Since, Bass suggests FDDI network. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a method and system having the different rate ports at a switch such gigabit Ethernet or Fibre channel as disclosed by Teitenberg's system into Bass and Hochschild's system. The motivation would have been to interface between the fast network with low speed network.

23. Claim 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hochschild (USP 5546391) in view of Holt (USP 5790545).

Regarding claim 55, Hochschild discloses (Figs 1,10 and col. 1, lines 12 to col. 28, lines 17) a network switch (Fig 3) comprising a plurality of input ports configured to receive data forming one or more packets (Fig 3A, Ref 310); a plurality of output ports configured to convey the packets out of the switch (Fig 3A, 380); a random access memory (Fig 3A, Ref 350); and data transport logic coupled between the input ports, the output ports, and the memory (Fig 3A, Ref 315, 312, 360), wherein a first input port is configured to request cut-through routing from at

least one destination output port in response to receiving data corresponding to a first packet that is a candidate for cut-through routing, wherein the destination output port is configured to convey a signal granting cut-through to the first input port if the destination output port has sufficient resources available to handle the data corresponding to the first packet, wherein, in response to receiving the grant cut-through signal, the input port is configured to route the data corresponding to the first packet to the destination output port via the data transport logic (Col. 12, lines 47 to col. 13, lines 44, the input port receives a packet and generates a request for forwarding the packet to output port; after receiving a grant signal from output port, the receiver will route the packet via a crosspoint switch to the output port by bypass the central queue), and wherein in response to not receiving the grant cut-through signal, the input port is configured to store the data to the shared memory via the data transport logic (Col. 13, lines 45-51, the input port does not receive a grant signal will forward the packet to the central queue), wherein the output port is configured to read the data corresponding to the first packet from the shared memory via the data transport logic in response to having resources available for the data corresponding to the first packet (Col. 13, lines 52-64, the output port will read the stored data in the central queue when it is available; col. lines 57-59). However, Hochschild fails to disclose input port configured to store packet identifier in the output port includes queues. In the same field of endeavor, Holt discloses a switch includes input port configured to store a packet tag in one of output port queues (Col. 5, lines 20-25).

Since Hochschild suggests that the switch which includes buffer at input port for allowing the upstream circuit and crossbar switch to operate at different speed. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made

to apply a method for configuring the input port for storing the packet tag in one of output port queues as disclosed by Holt into Hoshschild's method and system. The motivation would have been to provide a simultaneous cut through and store and forward frame in a network device to improve transmission delay.

24. Claims 57-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hochschild (USP 5546391) in view of Egbert (USP 6091707).

Regarding claims 57-59, Hochschild discloses (Figs 1,10 and col. 1, lines 12 to col. 28, lines 17) a network switch (Fig 3) comprising a plurality of input ports configured to receive data forming one or more packets (Fig 3A, Ref 310); a plurality of output ports configured to convey the packets out of the switch (Fig 3A, 380); a random access memory (Fig 3A, Ref 350); and data transport logic coupled between the input ports, the output ports, and the memory (Fig 3A, Ref 315, 312, 360), wherein a first input port is configured to request cut-through routing from at least one destination output port in response to receiving data corresponding to a first packet that is a candidate for cut-through routing, wherein the destination output port is configured to convey a signal granting cut-through to the first input port if the destination output port has sufficient resources available to handle the data corresponding to the first packet, wherein, in response to receiving the grant cut-through signal, the input port is configured to route the data corresponding to the first packet to the destination output port via the data transport logic (Col. 12, lines 47 to col. 13, lines 44, the input port receives a packet and generates a request for forwarding the packet to output port; after receiving a grant signal from output port, the receiver will route the packet via a crosspoint switch to the output port by bypass the central queue), and wherein in response to not receiving the grant cut-through signal, the input port is configured to

store the data to the shared memory via the data transport logic (Col. 13, lines 45-51, the input port does not receive a grant signal will forward the packet to the central queue), wherein the output port is configured to read the data corresponding to the first packet from the shared memory via the data transport logic in response to having resources available for the data corresponding to the first packet (Col. 13, lines 52-64, the output port will read the stored data in the central queue when it is available; col. lines 57-59). However, Hochschild fails the destination output port is configured to ensure that a sufficient amount of data from the packet has been stored into the shared memory before starting to read the data corresponding to the first packet from memory, thereby preventing an output underrun. In the same field of endeavor, Egbert discloses a method and system for prevent an underrun of a memory by setting a threshold value in order to compare with the amount stored data before transferring the data (Fig 4 and Col. 11, lines 25-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a method for preventing an underrun of a memory by setting a threshold value in order to compare with the amount stored data before transferring the data as disclosed by Egbert into Hochschild. the motivation would have been to improve the throughput of the network.

25. Claims 41-44, 47-48, 51-52, 54 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kotzur (USP 6094434) in view of Holt (USP 5790545).

Regarding claims 41-44 and 61, Kotzur discloses a network switch comprising a plurality of ports, wherein a first one of said ports is an input port configured to receive data forming a packet, wherein a second one of said ports is an output port configured to convey the packet out

of the switch (Fig 1), wherein the output port comprises an output first-in first-out memory (Fig 3A or Fig 4); a random access memory (fig 2, Ref 212); and a means for routing the data between the input port, the RAM, and the output port (Fig 2, Ref 220 and 210), wherein the means for routing is configured to either route the packet directly to the output FIFO by cut-through routing or route the packet to the RAM for either early forwarding or store and forward routing (Fig 12A, Ref 1224, store and forward or cut-through); wherein the routing means is configured to determine whether the output FIFO has sufficient storage available to store the packet (Fig 12A, Ref 1208 and 1225), wherein the means is configured to route the data from the input port to the output port in response to detecting that the output FIFO has resources available for the packet (Fig 12A, Ref 1233, Fig 12B, 1264), wherein the means is configured to store the data to the RAM in response to detecting that the output FIFO does not have room available for the packet (Fig 12A, 1208, 1226) , and wherein, in response to detecting that the output FIF'O has room available to store the packet after at least a portion of the data has already been stored in the RAM, the means is configured to forward the stored data to the output FIFO (Fig 12B). Kotzur fails to fully disclose input port configured to store packet identifier in the output port includes queues. In the same field of endeavor, Holt discloses a switch includes input port configured to store a packet tag in one of output port queues (Col. 5, lines 20-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a method for configuring the input port for storing the packet tag in one of output port queues as disclosed by Holt into Kotzur's method and system. The motivation would have been to provide a simultaneous cut through and store and forward frame in a network device to improve transmission delay.

Regarding claims 47-48, 51-52 and 54, Kotzur and Holt fails to disclose the claimed invention. However, the examiner takes an official notice that a method and system comprise the output port comprises control logic and an availability register, wherein the availability register is configured to store a value that the control logic compares with the amount of storage available in the output FIFO to determine if a signal granting cut-through should be transmitted to the input port; means for delaying the forwarding of the stored data to the output FIFO until the RAM has received enough of the packet to ensure that the output port will not underflow; storing the packet to the RAM by allocating clusters and cells to the packet; switch is configurable to selectively disable cut-through routing and early forwarding are well known and are well known and expected in the art. Therefore, it would have been obvious to one of ordinary skill in the art to implement the method and system as discussed above into the teaching of Kotzur and Holt. The motivation would have been to reduce the cost of the system.

26. Claim 62 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kotzur (USP 6094434) in view of Egbert (USP 6091707).

Regarding claim 62, Kotzur discloses a network switch comprising a plurality of ports, wherein a first one of said ports is an input port configured to receive data forming a packet, wherein a second one of said ports is an output port configured to convey the packet out of the switch (Fig 1), wherein the output port comprises an output first-in first-out memory (Fig 3A or Fig 4); a random access memory (fig 2, Ref 212); and a means for routing the data between the input port, the RAM, and the output port (Fig 2, Ref 220 and 210), wherein the means for routing is configured to either route the packet directly to the output FIFO by cut-through routing or route the packet to the RAM for either early forwarding or store and forward routing (Fig 12A,

Ref 1224, store and forward or cut-through); wherein the routing means is configured to determine whether the output FIFO has sufficient storage available to store the packet (Fig 12A, Ref 1208 and 1225), wherein the means is configured to route the data from the input port to the output port in response to detecting that the output FIFO has resources available for the packet (Fig 12A, Ref 1233, Fig 12B, 1264), wherein the means is configured to store the data to the RAM in response to detecting that the output FIFO does not have room available for the packet (Fig 12A, 1208, 1226) , and wherein, in response to detecting that the output FIF'O has room available to store the packet after at least a portion of the data has already been stored in the RAM, the means is configured to forward the stored data to the output FIFO (Fig 12B). Kotzur fails to fully disclose fails the destination output port is configured to ensure that a sufficient amount of data from the packet has been stored into the shared memory before starting to read the data corresponding to the first packet from memory, thereby preventing an output underrun. In the same field of endeavor, Eghert discloses a method and system for prevent an underrun of a memory by setting a threshold value in order to compare with the amount stored data before transferring the data (Fig 4 and Col. 11, lines 25-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a method for preventing an underrun of a memory by setting a threshold value in order to compare with the amount stored data before transferring the data as disclosed by Eghert into Kotzur. the motivation would have been to improve the throughput of the network.

Allowable Subject Matter

4. Claims 63-65 are allowed.

28. Claims 56 and 60 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

29. Claims 17 and 38 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

27. Claims 49-50 and 53 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven HD Nguyen whose telephone number is (571) 272-3159. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D. Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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7/9/05